CLAIMS:

1. A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage coupled between a supply voltage source and a reference voltage source; and

driving a gate terminal of least one element of said output stage to a level above that of said supply voltage source or below that of said reference voltage source in said Sleep Mode of operation.

2. The power-gating technique of claim 1 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source.

3. The technique of claim 2 wherein said gate terminal of said N-channel transistor is driven below said reference voltage level while in said Sleep Mode of operation.

4. The technique of claim 2 wherein said gate terminal of said P-channel transistor is driven above said supply voltage level while in said Sleep Mode of operation.

5. A circuit comprising:

an output stage comprising first and second series coupled transistors coupled between a supply voltage source and a reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage

level to a gate terminal of said first transistor greater than that of said supply voltage source in response to a Sleep Mode of operation.

6. The circuit of claim 5 wherein said output stage comprises a CMOS inverter and said first transistor comprises a P-channel transistor.

7. The circuit of claim 5 wherein said voltage level applied to said gate terminal of said first transistor comprises substantially said supply voltage source level plus 0.3V.

8. A circuit comprising:

an output stage comprising first and second series coupled transistors coupled between a supply voltage source and a reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage level to a gate terminal of said second transistor lesser than that of said reference voltage source in response to a Sleep Mode of operation.

9. The circuit of claim 8 wherein said output stage comprises a CMOS inverter and said second transistor comprises a N-channel transistor.

10. The circuit of claim 8 wherein said voltage level applied to said gate terminal of said second transistor comprises substantially said reference voltage source level minus 0.3V.

11. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a supply voltage source and a power-gated reference voltage line;

an output stage coupled between said supply voltage source and a reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to a stage preceding said output stage for driving said input to a level lower than that of said reference voltage source level in response to a Sleep Mode of operation.

12. The integrated circuit device of claim 11 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

13. The integrated circuit device of claim 12 wherein a gate terminal of said at least one N-channel transistor is driven to establish a negative V_{GS} in response to said Sleep Mode of operation.

14. An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a reference voltage source and a power-gated supply voltage line;

an output stage coupled between a supply voltage source and said reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to said input of said output stage for driving said input to a level higher than that of said supply voltage source level in response to a Sleep Mode of operation.

15. The integrated circuit device of claim 14 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

16. The integrated circuit device of claim 15 wherein a gate terminal of said at least one P-channel transistor is driven to a level greater than a threshold voltage above a level of said supply voltage source in response to said Sleep Mode of operation.